In the Claims

Claim 1 (previously presented): A semiconductor processing method of forming integrated circuitry comprising:

forming memory circuitry and peripheral circuitry over a substrate, the peripheral circuitry comprising first and second type MOS transistors; and

conducting second type halo implants into the first type MOS transistors in less than all peripheral MOS transistors of the first type, wherein the conducting of the second type halo implants includes conducting said implants into only one of the source and drain regions in less than all of the peripheral MOS transistors of the first type, and not the other of said source and drain regions of said less than all of the peripheral MOS transistors of the first type.

Claim 2 (original): The semiconductor processing method of claim 1, wherein the second type is p-type.

Claim 3 (cancelled).

Claim 4 (cancelled).

Claims 5-15 (cancelled).

Claim 16 (withdrawn): A semiconductor processing method comprising:

a masking step providing a common mask; and

an implant step carried out through the common mask, comprising conducting a halo implant of devices formed over a substrate comprising memory circuitry and peripheral circuitry sufficient to impart to at least three of the devices three different respective threshold voltages, at least some of the devices forming memory access devices.

Claim 17 (withdrawn): The method of claim 16, wherein the at least some of the devices forming memory access devices receive halo implants on a bit line contact side of the devices.

Claims 18-40 (cancelled).

Claim 41 (withdrawn): A method of improving DRAM storage cell retention time comprising conducting, in a common masking step and in a common implant step, a halo implant of devices formed over a substrate comprising memory circuitry and peripheral circuitry sufficient to impart to each device one of two or more different respective threshold voltages, at least some of the devices forming memory access devices, wherein the at least some of the devices forming memory access devices receive halo implants on a bit line contact side of the devices.

Claim 42 (withdrawn): The method of claim 41 wherein the halo implant is performed prior to formation of sidewall spacers in the memory access devices.

Claim 43 (withdrawn): The method of claim 41 wherein the halo implant is performed after formation of sidewall spacers in the memory access devices.

Claim 44 (withdrawn): The method of claim 41 wherein the halo implant is accompanied with an n-minus implant on the bit line contact side.

Claim 45 (withdrawn): The method of claim 41 wherein the storage node side of the memory access device is masked from the halo implant.

Claim 46 (withdrawn): A method of improving DRAM storage cell retention time comprising forming memory access devices having different implants and hence different junction structures on a bit line contact side and a storage node side respectively.

Claim 47 (withdrawn): The method of claim 46 wherein forming memory access devices includes:

performing, during a masking and implant step, a one-sided halo implant on the bit line contact side; and

performing, during the masking and implant step, an n-minus implant on the bit line contact side.

Claim 48 (withdrawn): The method of claim 47, wherein performing a one-sided halo implant is performed prior to formation of sidewall spacers.

Claim 49 (withdrawn): The method of claim 46, wherein the storage node side is masked during a one-sided halo implant on the bit line contact side.

Claim 50 (New): The semiconductor processing method of claim 1, wherein the peripheral MOS transistors are formed over a planar upper surface of the substrate, and wherein the conducting of the second type halo implants comprises angled implants relative the planar upper surface of the substrate.

Claim 51 (New): The semiconductor processing method of claim 1, wherein the drain regions are formed by an out-diffusion process.

Claim 52 (New): The semiconductor processing method of claim 1, wherein the drain regions are formed by an implant process that does not employ a masking step.

Claim 53 (New): The semiconductor processing method of claim 1, wherein at least a portion of the source regions are formed by an implant process that does not employ a masking step.

Claim 54 (New): The semiconductor processing method of claim 1, wherein the conducting of the second type halo implants comprises partially masking the less than all of the peripheral MOS transistors of the first type.

Claim 55 (New): The semiconductor processing method of claim 1, wherein the conducting of the second type halo implants into the one of the source and drain regions comprises masking a portion of the one of the source and drain regions.

Claim 56 (New): The semiconductor processing method of claim 1, wherein the conducting of the second type halo implants into the one of the source and drain regions comprises masking a majority portion of the one of the source and drain regions.

Claim 57 (New): The semiconductor processing method of claim 1, wherein the conducting of the second type halo implants into the one of the source and drain regions comprises masking an entirety of the one of the source and drain regions.